**PVP 20**

Code: 20CS3301, 20IT3301

**II B.Tech - I Semester – Regular / Supplementary Examinations**
**DECEMBER 2022**

# FUNDAMENTALS OF DIGITAL LOGIC DESIGN

**(Common for CSE, IT)**

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

BL – Blooms Level CO – Course Outcome

| | | | BL | CO | Max. Marks |
|---|---|---|---|---|---|
| **UNIT-I** | | | | | |
| 1 | a) | Solve the binary arithmetic operations on (-14) - (-2) using signed 2's complement representation. | L3 | CO1 | 7 M |
| | b) | Determine the equivalent number in base 10, base 3, base 16 and base 2 of a given number $(127.75)_8$ . | L3 | CO1 | 7 M |
| **OR** | | | | | |
| 2 | a) | Use 2's complement form to deduct.<br>i) 1101010 - 110100<br>ii) 10011.1101 - 101.11 | L3 | CO1 | 7 M |
| | b) | Find the following to the required form.<br>i) $(A98B)_{12}$ = (---------)$_3$<br>ii) $(38.65)_{10}$ = (----------)$_2$ | L3 | CO1 | 7 M |

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| **UNIT-II** | | | | | |
| 3 | a) | State and Prove the Huntington postulates of Boolean Algebra. | L3 | CO2 | 7 M |
| | b) | Simplify the following expression to sum of products using Tabulation Method:<br>$F(a, b, c, d) = \sum m(0,4,8,10,12,13,15) + d(1,2)$ | L3 | CO2 | 7 M |
| **OR** | | | | | |
| 4 | a) | Reduce the following Boolean expressions using theorems and identities.<br>i) F = C + AB + AD(B + C )+ CD<br>ii) F = AB + CDB + ACD | L3 | CO2 | 7 M |
| | b) | Simplify the following expression using the K-map:<br>Y = A'B'C'+ AC'D' + AB'+ ABCD' + A'B'C | L3 | CO2 | 7 M |
| **UNIT-III** | | | | | |
| 5 | a) | Draw the logic circuit of a 3 to 8 decoder and explain its working. | L2 | CO3 | 7 M |
| | b) | Explain the working of a De-multiplexer with the help of an example. | L2 | CO3 | 7 M |
| **OR** | | | | | |
| 6 | a) | Design a Full Adder circuit using Decoder and logic gates. | L3 | CO3 | 7 M |
| | b) | Discuss in detail about the design procedure for 4 bit binary parallel adder with diagram. | L3 | CO3 | 7 M |

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| **UNIT-IV** | | | | | |
| 7 | a) | Explain how to convert S-R flip flop into JK-flip flop. Draw and explain the logic diagram. | L3 | CO4 | 7 M |
| | b) | Develop the characteristic equation for JK-flip flop. | L3 | CO4 | 7 M |
| **OR** | | | | | |
| 8 | a) | Explain how to convert SR flip-flop to T flip-flop. | L2 | CO4 | 7 M |
| | b) | Construct a JK flip-flop using D flip-flop, multiplexer and an inverter. | L4 | CO4 | 7 M |
| **UNIT-V** | | | | | |
| 9 | a) | Explain the operation of 4 bit universal shift register with a neat logic diagram. | L2 | CO5 | 7 M |
| | b) | Write the differences between synchronous and asynchronous counters. | L3 | CO5 | 7 M |
| **OR** | | | | | |
| 10 | a) | Design a synchronous counter to generate the sequence 0,1,2,3,5,8… and repeat the sequence using T flip-flops. | L4 | CO5 | 7 M |
| | b) | Write the characteristic, excitation tables for JK, RS, T and D flip-flops. | L3 | CO5 | 7 M |